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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,456	02/19/2002	Akira Yoshida	NIT-329	9874

7590 05/19/2004

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EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	7

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/076,456	YOSHIDA ET AL.	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *27 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 7 .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-12 are pending in the application.

Claims 1-12 are rejected.

2. The status of claims 1-12 are incorrectly stated in the supplemental amendment filed on 27 February 2004 (Paper No. 6) as "Previously Presented" or "Original", however the claims are amended. Examiner has changed their status to "Currently Amended".

Response to Amendment

3. Applicant's amendments filed on 24 February 2004 (Paper No. 3) and 27 February 2004 (Paper No. 6) in response to the office action mailed on 24 November 2003 necessitate new ground(s) of rejection under 35 U.S.C. 103(a) as presented below in this Office action.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

5. The drawings filed on 24 February 2004 have been approved by the Examiner.

Claim Objections

6. Claims 1-12 are objected to because of the following informalities:

The phrase "said first disk array controlling unit" (Claim 1, lines 19-20; claim 7, lines 22-23) is improper because a singular disk array controlling unit has not been previously recited in the claims. It is suggested that this phrase be replaced by the phrase "a first disk array controlling unit". The claim(s) will be interpreted in light of this suggestion.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-3 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (EP 1,132,805 A2) in view of Obara (JP 11-296313 A).

As in claim 1, Fig. 1 of Fujimoto describes a disk array controller comprising:

a plurality of disk array controlling units comprising a channel interface section, a disk interface section connected to a magnetic disk unit and a cache memory section that temporarily stores data as read out of or written into the magnetic disk unit (Figs. 1 and 7, elements 1-1, 11, 12 and 14; column 7, line 58 to column 8, line 14); and

a mutual connection network in connection with the channel interface sections, the disk interface sections and the cache memory sections of the disk array controlling units (Fig. 1, element 220; column 8, lines 5-14);

wherein the cache memory sections perform a transfer of the data with the channel interface sections of the disk array controlling units (Column 8, lines 33-47),

wherein in case of transferring a copy of data stored in the magnetic disk unit which is associated with a first disk array controlling unit included in the plurality of disk array controlling units, from the first disk array controlling unit to a second disk array controlling unit included in the plurality of disk array controlling units, the first disk array controlling unit performs a transfer of the copy of data via the mutual connection network (Column 11, lines 14-25; column 11, line 45 to column 12, line 9).

The disk array controller described in Fig. 1 of Fujimoto does not include a host switch interface section connected to a host computer and interfacing with the host switch interface sections of the disk array controlling units as required by claim 1.

The disk array controller described in Fig. 1 of Fujimoto also does not teach that the host switch interface section selects a relay destination for data sent from the host to the first disk array controlling unit, from the channel interface section in the first, second or another disk array controlling unit in accordance with operational conditions of the first, second and another disk array controlling units, as also required by claim 1.

Obara teaches a method of load balancing in a disk storage system, wherein a host (Fig. 4, element 1) is connected to a plurality of disk controllers (Fig. 4, elements 8a and 8b) through a switch (i.e. a host switch interface) (Fig. 4, element 21), and the relay destination (i.e. the disk controller) for accessing associated disk storage is selected from the plurality of disk controllers based on the load of the disk controllers (i.e. in accordance with operational conditions of the disk controllers) (Fig. 4; Abstract).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to interconnect the host computer and the channel interface sections of the disk array controlling units using a host switch interface, and to select a relay destination from a plurality of disk controllers based on the load of the disk controllers as taught by Obara, in the system taught in Fig. 1 of Fujimoto, in order to balance the loads of the disk controllers as taught by Obara.

As in claim 2, Obara teaches that the host switch interface section includes a management table (Fig. 4, element 29) that selects a data transfer path according to an address as requested by the host computer (Abstract), where it is noted that the combination of control unit number and volume number of a frame may be interpreted as an address.

Fig. 4 of Fujimoto describes a disk array controller comprising a plurality of disk array controlling units, where an interconnection between a host computer and the channel interface sections of the disk array controlling units operates as a switch (i.e. host switch interface section) (Fig. 4, element 23; column 3, line 55 to column 4, line 6), providing an equivalent function to the switch of Obara in that the host can be selectively connected to any disk controller (Column 3, line 55 to column 4, line 6).

Therefore, it would have been obvious to use a switch as in Fig. 4 of Fujimoto, in the system of Fig. 1 of Fujimoto, and to control the switch according to the load balancing of Obara, due to the similarity in the nature of the switch elements in Fig. 4 of Fujimoto and Obara, namely to provide a switching function between the host and the plurality of disk controllers.

As in claim 2, Fujimoto further describes that the host switch interface of Fig. 4 is provided with a map (i.e. management table) that selects a path of the data transfer according to an address as requested by the host computer (Column 3, line 55 to column 4, line 6), where it is readily apparent in Fujimoto that operating multiple disk array controllers as a single disk array controller implies that the host views the disk array as a continuous non-overlapping address

space, and the analysis of the access request from the host computer that allows designation of a particular disk array controller is a decoding of the address.

As in claim 3, Fujimoto teaches that the data transfer path selected by the host switch interface of Fig. 4 is a path between the host switch interface section and the channel interface sections of the disk array controlling units (Fig. 4, path connections between elements 23 and 11).

Claims 7-9 are rejected using the same rationale as for the rejection of claims 1-3 above, where it is noted that the second mutual connection network recited in claim 7 is intrinsic in the host switch interface of claim 1.

9. Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (EP 1,132,805 A2) in view of Obara (JP 11-296313 A) as applied to claims 2 and 8 above, and further in view of Fan (US Pub 2002/0054567).

Fujimoto and Obara are relied upon for the teachings relative to claims 2 and 8 as above.

The combination of Fujimoto and Obara does not teach that the management table includes path selection and volume history information, wherein candidates for the data transfer paths respond to an address and the specific path is selected on the basis of the volume history information as required by claims 4 and 10.

Fan teaches a dynamic load balancing method where a link table (i.e. management table) is provided for selecting a link (i.e. path) for data transmission between a switch and a server (Figs. 1 and 8; page 3, paragraph 59; page 6, paragraph 109). Fan teaches that the specific link is selected on the basis of an address by first associating an address with a flow (Fig. 8, step 820; page 6, paragraph 109, lines 5-8 and 27-35), where the flow is associated with a particular link based upon volume history information (Fig. 3; page 4, paragraphs 61-62; Fig. 8, steps 830 and 850; page 6, paragraph 109, lines 8-14; pages 6-7, paragraph 110). Fan teaches that this method effects dynamic load balancing of heterogeneous-speed links (Page 4, paragraph 61, lines 1-3).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to select the path for data transfer in response to an address and based on volume history information using the management table as taught by Fan, in the system made obvious by the combination of Fujimoto and Obara, in order to effect dynamic load balancing of heterogeneous-speed links as taught by Fan.

10. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (EP 1,132,805 A2) in view of Obara (JP 11-296313 A) as applied to claims 1 and 7 above, and further in view of Rakvic (US Pub 2002/0188804).

Fujimoto and Obara are relied upon for the teachings relative to claims 1 and 7 as above.

The combination of Fujimoto and Obara does not teach that one part of the disk array controlling units are provided with higher-speed cache memory sections than those of the other part as required by claims 5 and 11.

Rakvic teaches that a cache may be divided into a number of subcaches and that each subcache may have a different speed at which it operates (Page 2, paragraph 22). The concept of subcaches is analogous to the cache memory sections contained in the disk array controlling units recited in claims 5 and 11 since these caches are mutually connected. Rakvic also teaches that slower subcaches are typically cheaper to produce and that costs may be reduced by using one fast subcache along with other slower caches (Page 2, paragraph 22).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use caches of different speeds as taught by Rakvic in the system made obvious by the combination of Fujimito and Obara in order to reduce costs as taught by Rakvic.

11. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (EP 1,132,805 A2) in view of Obara (JP 11-296313 A) as applied to claims 2 and 8 above, and further in view of Fan (US Pub 2002/0054567) and Jantz (US 5,937,428).

Fujimoto and Obara are relied upon for the teachings relative to claim 2 and 8 as above.

The combination of Fujimoto and Obara does not teach that the disk array controlling units include a resource management section that manages an operating ratio of the resources and reports the operating ratio through a report signal to the host switch interface, and a management table including path selection and history information that includes weightings based on the report signal, wherein candidates for the data transfer paths respond to an address and the specific path is selected on the basis of the weighting in the history information as required by claims 6 and 12.

The rationale derived from Fan in the rejection of claims 4 and 10 above is incorporated herein for the teaching of a dynamic load balancing method where a link table (i.e. management table) is provided for selecting a link (i.e. path) for data transmission between a switch and a server, that the specific link is selected on the basis of an address by first associating an address with a flow, where the flow is associated with a particular link based upon volume history information, and that this method effects dynamic load balancing of heterogeneous-speed links.

Jantz teaches a disk array control system comprising a plurality of disk controllers where read access requests are dispatched to the controllers based upon a weight calculated from the previous commands to each controller (i.e. history information) (Fig. 5; column 10, lines 15-30). The weights (i.e. operating ratios) are managed in the controllers (Fig. 5, elements 122 and 132). It is readily apparent that the dispatcher must have access to the weight information through a signal (i.e. a report signal) in order to make a decision as to which controller to dispatch the next read access (Column 10, lines 23-26). Here the dispatcher may be viewed as having the same

functionality as the host switch interface. Jantz also teaches that this configuration more accurately balances the I/O load (Column 10, lines 30-36).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to select the path for data transfer in response to an address and based on history information using the management table of Fan, to manage an operating ratio of the resources and report the operating ratio through a report signal to the host switch interface as taught by Jantz, and to include in the history information weighting information as the basis for path selection as also taught by Jantz, in the system made obvious by the combination of Fujimoto and Obara, in order to effect dynamic load balancing of heterogeneous-speed links as taught by Fan and to more accurately balance the I/O load as taught by Jantz.

Response to Arguments

12. Applicant's arguments filed 24 February 2004 with respect to the rejection of claims 1 and 7 under 35 U.S.C. 103(a) have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMR

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